ABSTRACT OF THE INVENTION

Method and system for shorten time needed to test a semiconductor device having a plurality of memory circuits. The semiconductor device includes an address decoder for selecting a plurality of memory circuits and causing the memory circuits to perform a read/write operation. A comparator receives plural pieces of read data read from the plurality of memory circuits and compares the plural pieces of read data with one another. A processing unit compares one of the plural pieces of read data with write data. Using the comparison results of the comparator and the processing unit shorten the time needed to test the plurality of memory circuits.